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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,349	03/08/2001	Joel Page	1120-CA	4186

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	9

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/803,349	PAGE ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/08/01;5/10/01;6/17/01;10/1/02;7/5/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-16* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 13, the limitation "the cells" in line 1 lacks an antecedence basis because the cells of the serial data output register does not mention or disclose in its preceding claim. For examination purposes, the examiner considers the limitation as cells.

Thus, claim 14 is also rejected for being dependent upon the rejected base claim 13.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 4-7, 10-11, and 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Schreiber et al. (U.S. 6,456,219).

Re claim 1, Schreiber et al. disclose in Figure 5 a programmable integrated circuit (Figure 5 and col. 3 lines 53-64) comprising: a bus (links or connections that connect all the components together, e.g. 104); a processor (105), connected to bus, for performing digital filtering on digital signals (decimation filter as label in 105), a data interface (interface of 105 for receiving 104), connected to bus, for receiving external digital signals (103) having respectively different characteristics (inherently unexpected input signals) for filtering by processor (105), and a serial data output register (109), for receiving filtered digital signals from processor (105) and providing them to an output port (110A).

Re claim 4, Schreiber et al. further disclose in Figure 5 a serial control interface (109).

Re claim 5, Schreiber et al. further disclose in Figure 5 a serial peripheral interface (109).

Re claim 6, Schreiber et al. further disclose in Figure 5 a general purpose I/O interface (109).

Re claim 7, Schreiber et al. further disclose in Figure 5 processor is configured to provide programmable decimation and filtering (105 as label).

Re claim 10, Schreiber et al. further disclose in Figure 5 formed on an integrated circuit (100A).

Re claim 11, Schreiber et al. further disclose in Figure 5 integrated circuit includes a token input pin (110A as D_{in}) and a token output pin (110A as D_{out}).

Re claim 15, it is a method of designing claim of claim 1. Thus, claim 15 is also rejected under the same rationale as rejected in claim 1.

Re claim 16, it is a method of fabricating claim of claim 1. Thus, claim 15 is also rejected under the same rationale as rejected in claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-3, and 12 are rejected under 35 U.S.C. 103(a) as being obvious over Schreiber et al. (U.S. 6,456,219) in view of Fischer et al. (U.S. 6,167,415).

Re claim 2, Schreiber et al. do not disclose at least one test modulator connected to bus for generating a test signal having a controlled delay. However, Fischer et al. disclose in Figure 19 one test modulator connected to bus for generating a test signal (test pattern in Figure 19 and abstract lines 24-28) having a controlled delay. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a test modulator connected to bus for generating a test signal having a controlled delay as seen in Fischer et al.'s invention into Schreiber et al.'s

invention because it would enable to increase the stability, quality, and performance of the system.

Re claim 3, Schreiber et al. in view of Fischer et al. do not disclose the at least one test modulator is programmable to selectively generate a test signal using different algorithms. However, the examiner take an official notice that a test signal would be generate using different algorithms is known in the art (e.g. WGN/WAGN and speech...). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add one test modulator is programmable to selectively generate a test signal using different algorithms into Schreiber et al. in view of Fischer et al.'s invention because it would enable to increase the stability, quality, and performance of the system by testing different type of test signals.

Re claim 12, Schreiber et al. do not disclose the above integrated circuit serially connected from token output pin of one integrated circuit to token input pin of the next integrated circuit in which the token input pin of a first programmable digital filter is connected to a micro-controller and the token output pin of a last programmable digital filter is connected to said micro-controller. However, Fischer et al. disclose in Figures 3 and 5B a cascade of filters (360a or 360b wherein each of these boxes include several filters connected in series) that is serially connected from token output pin of one integrated circuit to token input pin of the next integrated circuit in which the token input pin of a first programmable digital filter is connected to a micro-controller and the token output pin of a last programmable digital filter (e.g. FIR filter is connected to IIR filter and than another FIR filter) is connected to said micro-controller. Therefore, it would

have been obvious to a person having ordinary skill in the art at the time the invention is made to add token output pin of one integrated circuit to token input pin of the next integrated circuit in which the token input pin of a first programmable digital filter is connected to a micro-controller and the token output pin of a last programmable digital filter is connected to said micro-controller as seen in Fischer et al.'s invention into Schreiber et al.'s into because it would enable to improve the system performance by having multiple filter for different signal characteristics.

7. Claims 9 and 13 are rejected under 35 U.S.C. 103(a) as being obvious over Schreiber et al. (U.S. 6,456,219).

Re claims 9 and 13, Schreiber et al. do not disclose in Figure 5 separate power supplies are provided respectively to data interface, processor, to serial data output register and the cells of the serial data output register not needed for delay are operated in a reduced power mode. However, the examiner takes an official notice that separate power supplies are provided respectively to data interface, processor, to serial data output register, and the cells of the serial data output register not needed for delay are operated in a reduced power mode are known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to have separate power supplies are provided respectively to data interface, processor, to serial data output register and the cells of the serial data output register not needed for delay are operated in a reduced power mode into Schreiber et al.'s invention because it would enable to stabilize the system by having separate power to each component, reducing the power

interference, and saving the system power by reducing power in component that is not in used.

Allowable Subject Matter

8. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claim 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,546,408 to Page et al. disclose a sinc filter using twisting symmetry.

b. U.S. Patent No. 6,321,246 to Page et al. disclose a linear phase fir sinc filter with multiplexing.

c. U.S. Patent No. 6,593,925 to Hakura et al. disclose a parameterized animation compression methods and arrangements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

June 23, 2004

ANIL KHATRI
PRIMARY EXAMINER